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TITLE

Unequal Error Protection Reed-Muller Code Generator and Decoder

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TITLE OF THE INVENTION

Unequal Error Protection Reed-Muller Code Generator and Decoder

BACKGROUND OF THE INVENTION

[0001] The present invention relates to unequal error protection block codes and more particularly to a generator matrix for an unequal error protection Reed-Muller code and a decoder for such code.

[0002] Error protection codes are well known in systems which transmit information from one point to another or which record data on a storage medium for later playback. For example, pictures taken by a space probe must be transmitted back to Earth over long distances and with low power. The signals are therefore subject to interference by noise sources which cause the signal received on Earth to be different from the transmitted signal. By proper encoding of the signal before transmission, it is possible to reconstruct the original signal from the corrupted signal actually received. In similar fashion, information written onto a storage medium such as a compact disk is subject to errors in the writing process, errors caused by damage and wear to the disk and errors in the reading process. These errors are like noise sources in a transmission channel. But, by encoding the information before writing it to the storage medium, a certain level of errors can be corrected when the information is read from the disk.

[0003] Information to be error protected is typically digitized and transmitted or stored as a series of binary digits, bits, represented as ones and zeros. Each unit or word of data is usually represented by a fixed series of bits, e.g. eight or sixteen bits. Error codes generally add bits to the length of the data words to

form code words which are transmitted or stored. For example, a repetition code may transmit or store a single "1" as four "1"s, which forms a 4,1 code (four bit codeword representing one bit of data). A decoder which receives a four bit word containing three "1"s and one "0" would assume that one error occurred and four "1"s were transmitted and would decode the received code word as a single data bit of "1".

[0004] Coding increases the reliability of transmitted data. But, coding increases the bandwidth needed to transmit a given amount of data. Stated differently, coding reduces the amount of data which can be transmitted with a given bandwidth. Much effort has been made to design codes which most efficiently use available bandwidth and achieve the best level of error protection.

[0005] In real systems, all data does not need the same level of error protection. For example, in error protecting voice or music, it is more important to ptotect the most significant bits than the least significant bits. In some forms of video compression, images are broken into blocks which are represented by a number of parameters, one of which is the scale factor which applies to all other bits in the block. Any error in the scale factor causes an error in all other bits in the block. Thus, it is more important to protect the scale bits than the other bits. In such cases, unequal error protection codes can be used to optimize the coding system by using relatively more bandwidth to protect the more important bits and relatively less to protect less important bits.

[0006] The Reed-Muller codes are known to be efficient error protecting codes. However, when signals are encoded with a standard Reed-Muller

generator matrix and decoded using standard algebraic decoding, the bit error rate for all bits is the same. It would be desirable to have a generator matrix for using Reed-Muller code to encode data with unequal error protection and a decoder which efficiently decodes the signals while maintaining the unequal error protection.

SUMMARY OF THE INVENTION

[0007] In accordance with the present invention, an unequal error protecting code is constructed by concatenating an original code with the sum of itself and a subcode of the original code. The resulting generator matrix provides unequal error protection. By proper decomposition, the generator matrix is simplified to a form which facilitates a simple decoding algorithm in which received code words are split into a plurality of parts which are decoded in parallel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1 is a block diagram of a signal transmission system with error protection coding.

[0009] Figure 2 is a block diagram of a signal decoder according to the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0010] Figure 1 illustrates a typical data transmission system in which the present invention is useful. Block 10 represents an input signal, for example a voice, music or picture signal which normally originates as an analog signal. For instance, the input signal may be the output of a microphone in a cellular telephone. At block 12, the analog signal from block 10 is converted from analog

to digital form. For example, an audio signal may be sampled and each sample may be represented by an eight or sixteen bit digital word. The digital signal from block 12 is coupled to an encoder 14 which provides forward error protection by converting each digital data word into a digital code word. The code words are then coupled to a transmitter 16 which may transmit the code words as radio frequency signals. The transmitted signals pass through a transmission channel 18, which may be the atmosphere of the Earth. Block 20 represents sources of noise or errors which cause the transmitted code words to be corrupted to some extent. At block 22, the transmitted signal plus noise are received and provided as a digital output to a decoder 24. The decoder 24 performs several functions. It detects errors in the received signal and, within certain limits, corrects the errors to identify the code word which was actually transmitted. When the proper codeword has been identified, it is mapped to the data word which would generate the code word in encoder 14. The digital data word is then coupled to a digital to analog converter 26 which may provide an analog output signal which is a good reproduction of the input signal from block 10.

[0011] As noted above, the system of Figure 1 may also represent a system which records and plays back an audio or video signal. The transmitter 16 may be a system for writing, or burning, data onto a CD or a DVD. The receiver 22 may be a CD or DVD player which reads the recorded information from the CD or DVD. The transmission channel may be the CD or DVD itself. The noise 20 is from errors in the writing process, reading process, and from scratches on the surface of the CD or DVD caused by improper handling.

[0012] In similar fashion, the transmission channel may be digital subscriber lines and/or long distance backbone telephone systems or the Internet. In the case of the Internet, the transmitter and receiver may be personal computer systems. Any such systems can be affected by noise sources and therefore can benefit from use of error protection coding. Such systems typically can optimize the tradeoff of bandwidth and error protection by use of unequal error protection codes.

[0013] The present invention provides a new method for designing an unequal error protecting code generator for encoder 14. It also provides a method for designing a corresponding decoder 24 which provides fast parallel decoding and maintains the unequal error protection. To clarify this disclosure of the present invention, only the case of binary codes and relatively short data and code words are considered.

[0014] The basic process for encoding a digital data word d into a block code word C is by use of a generator matrix G, according to the equation:

$$[d]\,[G] = [C]$$

The data word d is represented by a vector having a length k. The generator matrix G has k rows and n columns. The code words C have a length of n. As a starting point for the embodiment which is described in this disclosure, assume k is four and n is eight. The resulting generator equation then has the form:

$$[x\ x\ x\ x]\begin{bmatrix} x & x & x & x & x & x & x & x \\ x & x & x & x & x & x & x & x \\ x & x & x & x & x & x & x & x \\ x & x & x & x & x & x & x & x \end{bmatrix} = [x\ x\ x\ x\ x\ x\ x\ x]$$

In this embodiment each "x" represents a digital one or zero. The code, C, is the complete set of all code words which are generated by multiplying every possible data word, d, by the generator matrix, G. Since the data word in this embodiment has four bits, it has sixteen possible values. There are therefore sixteen code words in the code, C, out of the 256 possible eight-bit digital vectors.

[0015] In one embodiment of the present invention, a Reed-Muller block code generator matrix, G, which produces the code C is used as the starting point for designing an improved generator matrix. Any binary block code, C, has subcodes, one of which is represented here as C_1. A subcode may be generated by any linear combination of the rows of the original matrix G, which combination forms a subcode generator matrix G_1. The subcode C_1 has a number of rows k_1 which is less than k. In the present embodiment, we will pick k_1 to be two. As a result, the subcode generator matrix G_1 can encode only two data bits and the subcode C_1 includes only four code words. The generator matrix G_1 has the same number of columns as G and produces code words having a length of eight in this embodiment.

[0016] In the present invention, a new unequal error protection code C_2 is generated by concatenating the original code C generated by matrix G with the sum of the same code and the subcode C_1 generated by matrix G_1. This process is represented by the equation:

$$C_2 = | U | U+V |$$

where U is a code word of C and V is a codeword of C_1. The new generator matrix G_2 for code C_2, is represented by the equation;

$$[G_2] = \begin{matrix}[G & G] \\ [0 & G_1]\end{matrix}$$

[0017] The generator matrix G_2 has more rows and more columns than matrix G. The additional rows are provided by G_1, which for this embodiment has two rows. G_2 therefore has six rows and can encode a data word of six bits. The matrix G_2 has sixteen columns and therefore generates code words which are sixteen bits long. In this embodiment, there are 64 code words in code C_2, one for each of the possible six bit data words.

[0018] Since C_1 is a subcode of C, we have the following coset decomposition of C:

$$C = C_1 + [C / C_1]$$

where $[C / C_1]$ denotes the sets of representatives of the cosets of C_1 in C. The generator matrix for the $[C / C_1]$ coset code is represented as G_3. The dimension, i.e. number of rows, of G_3 is k_3 which is equal to k minus k_1. Therefore, the generator matrix G for code C may be represented as:

$$[G] = \begin{matrix}[\ G_3\ ] \\ [\ G_1\ ]\end{matrix}$$

[0019] The generator matrix G_2 for code C_2 may therefore be rewritten as:

$$[G_2] = \begin{matrix}[G_3 & G_3] \\ [G_1 & G_1] \\ [0 & G_1]\end{matrix}$$

[0020] The linear operation of subtraction of one row from another does not change the nature of a code generator matrix. Therefore, by subtracting the last two rows of G_2 from the middle two rows of G_2, the matrix G_2 may also be rewritten as:

$$[G_2] = \begin{matrix}[G_3 & G_3] \\ [G_1 & 0] \\ [0 & G_1]\end{matrix}$$

[0021] In the present embodiment, each of the submatrices G_3 and G_1 have two rows and generator matrix G_2 has a total of six rows. The generator matrix G_2, is therefore designed to encode six bit words instead of the original four-bit data word d. The data vector d_2 for our new code C_2 is six bits long, four corresponding to the original code C and two corresponding to the subcode C_1. The data word d_2 can be divided into three parts for further explanation of the present invention as follows:

$$[d_2] = [\, d_a \mid d_b \mid d_c \,]$$

The new code C_2 is generated according to the following equation:

$$[\, d_a \mid d_b \mid d_c \,] \times \begin{matrix}[G_3 & G_3] \\ [G_1 & 0] \\ [0 & G_1]\end{matrix} = [\, C \mid C + C_1 \,] = [C_2]$$

[0022] From this equation, several things can be seen. The lengths of data bits d_a, d_b, and d_c are k_3, k_1, and k_1 respectively. Data bits d_a affect both halves of the code words C_2 and should therefore have increased error protection. Data bits d_a and d_b generate the left half of the code words C_2. Data bits d_a and d_c generate the right half of the code words C_2. The decomposition of the generator matrix G_2 to include the two zero or empty submatrices provides this separation

of the right and left halves of the code word and simplifies decoding as explained below. In the present embodiment, data word d_2 is six bits long and therefore has 64 possible values. Therefore, there are 64 code words in C_2.

[0023] In the embodiment which has been described above, the encoder 14 receives six bit digital words and generates sixteen bit code words for transmission by transmitter 16. When receiver 22 receives the transmitted signals corrupted by noise source 20, it will produce sixteen bit received signal vectors y which include errors and therefore do not exactly match any of the allowable code words in C_2. A standard decoding technique is to find the code word C_2 which has the minimum squared Euclidean distance D to the vector y. This may be expressed as:

$$D = \sum (y_i - c_i)^2$$

[0024] A straightforward way to do this is the exhaustive search approach. This involves calculating the distance D from every allowable code word C_2 to each received signal vector y, comparing the values of D and selecting the codeword C_2 having the smallest value as the correct code word. The data word which corresponds to the selected code word would then be selected as the transmitted data word. In the present embodiment having sixty-four sixteen-bit code words, the exhaustive search approach would require making sixty-four distance calculations of sixteen bit words and comparing the sixty-four results to find the smallest. It can be seen that a considerable amount of hardware may be required to perform such a decoding function and it could slow overall system operating speed. As the data word size is increased and the code word size is

increased proportionally, the exhaustive search approach requires dramatically more hardware and can cause unacceptable time delays in decoding.

[0025] The codes generated according to the present invention allow the decoding process to be broken down into smaller decoding steps which may be performed in parallel, i.e. simultaneously. The result is that less hardware and time are required.

[0026] The received signal vector, y, provided by receiver 22 is first broken into left and right halves, y_L, and y_R. In the present embodiment where each code word C_2 is sixteen bits long, each half word is therefore eight bits long. The left code words are from the code word set C and the right code words are from the code word set $C + C_1$. Due to the way the generator matrix G_2 has been designed, each half of the received signal y may be decoded independently of the other and therefore may be decoded simultaneously.

[0027] Figure 2 is a block diagram of a simplified decoder made possible by the present invention and illustrates the parallel nature of the decoder. In Figure 2 there are four decoder sections 30, 32, 34, 36, each of which is also identified by the letters A, B, C, and D respectively. Decoder section 30 includes a left half decoder unit A (LHDU-A) 38 and a right half decoder unit A (RHDU-A) 40. In similar fashion, decoder section 32 includes left and right half decoder units 42, 44; decoder section 34 includes left and right half decoder units 46, 48; and decoder section 36 includes left and right half decoder units 50, 52. The received signal left half, y_L, is coupled to each of the left half decoders 38, 42, 46, and 50. The received signal right half, y_R, is coupled to each of the right half

decoders 40, 44, 48, and 52. The outputs of the two halves 38, and 40 of decoder section 30 are coupled to an adder 54. In similar fashion, adders 56, 58 and 60 are provided to add the right and left half signals for each of the decoder sections 32, 34 and 36. The outputs of all adders 54, 56, 58 and 60 are coupled to a comparator 62.

[0028] In the present embodiment, four decoder sections are used because the first part d_a of the data word d_2 has a length of two bits. Therefore d_a has four possible digital values: 00, 01, 10 and 11. Each of the four data sections assumes one of these four values and decodes for the other possible values of the right and left halves of the code words.

[0029] LHDU-A 38 assumes that the value of d_a is 00 and finds the value of d_b which minimizes the value of the distance D:

$$D = \| y_L - C \|^2 = \| y_L - [\, 00 \mid d_b \,] \begin{matrix} [\, G_3 \,] \\ [\, G_1 \,] \end{matrix} \|^2$$

[0030] LHDU-B 42 assumes that the value of d_a is 01 and finds the value of d_b which minimizes the value of:

$$D = \| y_L - C \|^2 = \| y_L - [\, 01 \mid d_b \,] \begin{matrix} [\, G_3 \,] \\ [\, G_1 \,] \end{matrix} \|^2$$

[0031] LHDU-C 46 assumes that the value of d_a is 10 and finds the value of d_b which minimizes the value of:

$$D = \| y_L - C \|^2 = \| y_L - [\, 10 \mid d_b \,] \begin{matrix} [\, G_3 \,] \\ [\, G_1 \,] \end{matrix} \|^2$$

[0032] LHDU-D 50 assumes that the value of d_a is 11 and finds the value of d_b which minimizes the value of:

$$D = || y_L - C ||^2 = || y_L - [11 | d_b] \begin{matrix} [G_3] \\ [G_1] \end{matrix} ||^2$$

Since d_b is two bits long, it has four possible values. Each of these comparisons therefore require comparison of only four eight-bit code words to the left half of the received signal vector. Note that C is a code word of the original code word set and therefore has a length of eight bits in this embodiment. Each of the decoder units 38, 42, 46 and 50 may perform its four distance calculations and selection of the smallest distance simultaneously. The outputs of each of these left half units includes the minimum calculated distance and the identity of the particular d_b which corresponds to the calculated distance.

[0033] RHDU-A 40 assumes that the value of d_a is 00 and finds the value of d_c which minimizes the value of D:

$$D = || y_R - [C + C_1] ||^2 = || y_R - [00 | d_c] \begin{matrix} [G_3] \\ [G_1] \end{matrix} ||^2$$

[0034] RHDU-B 44 assumes that the value of d_a is 01 and finds the value of d_c which minimizes the value of:

$$D = || y_L - [C + C_1] ||^2 = || y_R - [01 | d_c] \begin{matrix} [G_3] \\ [G_1] \end{matrix} ||^2$$

[0035] RHDU-C 48 assumes that the value of d_a is 10 and finds the value of d_c which minimizes the value of:

$$D = || y_L - [C + C_1] ||^2 = || y_L - [10 | d_c] \begin{matrix} [G_3] \\ [G_1] \end{matrix} ||^2$$

[0036] RHDU-D 52 assumes that the value of d_a is 11 and finds the value of d_c which minimizes the value of:

$$D = || y_L - [C + C_1] ||^2 = || y_L - [11 \mid d_c] \begin{bmatrix} G_3 \\ G_1 \end{bmatrix} ||^2$$

[0037] Since d_c is two bits long, it has four possible values. Each of these comparisons therefore require comparison of only four eight-bit code words to the right half of the received signal vector. Each of the decoder units 40, 44, 48 and 52 may perform its four distance calculations and selection of the smallest distance simultaneously and at the same time the left half calculations are made. The outputs of each of these right half units includes the minimum calculated distance and the identity of the particular d_c which corresponds to the calculated distance.

[0038] In the present embodiment, it should be noted that the right half and left half decoder units, e.g. 38 and 40, are identical. The data word sections d_b and d_c are each two bits long and therefore have the same four possible digital values. Both d_b and d_c are multiplied by subcode generator matrix [G_1], to determine the possible code words for the distance D calculation.

[0039] As shown in Figure 2, the left and right half outputs for each decoder section 30, 32, 34 and 36 are combined in adders 54, 56, 58 and 60. The adders sum the smallest distances D calculated in each pair of decoder units and couple the sums to comparator 62. Comparator 62 picks the smallest input to identify the correct codeword and transmitted data word for the received signal vector y.

Since each decoder section 30, 32, 34 and 36 corresponds to one of the four possible values of d_a, the comparator 62 automatically knows the proper value for d_a. That is, if the output of adder 56 is the smallest, the value of d_a is 01. In addition to providing the distance values D, each of the decoder sections keeps track of the values of d_b and d_c which correspond to the smallest D values calculated. When comparator 62 picks the section with the smallest combined D value, it therefore also picks the values of d_b and d_c identified by the respective decoder unit as the proper data word values. The combined d_a, d_b and d_c is therefore picked as the correct transmitted data word d_2 and is provided on output 64, which is coupled to the input of digital to analog converter 26 of Figure 1.

[0040] In the above-described process of designing a new generator matrix from an existing block code, a decomposition process was used once. That is, a subcode of the original code was selected and concatenated with the original code. The decomposition process can be applied again to the new generator matrix G_2 one or more times. That is, a subcode of G_2 may be selected and concatenated with G_2 and decomposed as described above. For each application of the decomposition process, further levels of unequal error protection may be provided and the decoding process can be decomposed into more levels of parallel decoding. In the embodiment described herein, each half decoding unit, e.g. 38, is required to make only four distance D calculations and pick the smallest as its output. If the length of the data word, and corresponding code word, is increased, the number of calculations and comparisons increases.

According to the present invention, the number of decompositions of the generator matrix is also increased to keep the number of distance calculations required by each data unit to a small value to speed the decoding process.

[0041] While the present invention has been illustrated and described in terms of particular apparatus and methods of use, it is apparent that equivalent parts and steps may be substituted for those shown and other changes can be made within the scope of the present invention as defined by the appended claims.